AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (canceled)

2. (currently amended) The layout of the semiconductor integrated circuit according to claim 31, wherein at least one of said power supply lines extends to be connected to an external connection terminal.

3. (currently amended) The layout of the semiconductor integrated circuit according to claim 31, further comprising a mutual connection line for connecting together some of said power supply lines having equal potentials, wherein the mutual connection line is not connected to any of said power supply lines other than those having equal potentials.

4. (currently amended) The layout of the semiconductor integrated circuit according to claim 31, wherein the area occupied by all of said power supply lines is larger than the area occupied by all of the regions between said power supply lines.

5. (withdrawn/ currently amended) The layout of the semiconductor integrated circuit according to claim 31, further comprising a gate signal wiring line in order to avoid a delay of a gate signal propagating through the corresponding one of the gate electrodes of said transistors, the gate signal wiring line having a resistance and a parasitic capacitance lower than those of the gate electrode.

6. (canceled)

7. (canceled)

8. (withdrawn) A charge pump circuit comprising the semiconductor integrated circuit according to claim 31, and a configuration of a plurality of capacitors and a plurality of transistors.

9-30. (canceled)

31. (currently amended) A layout of a semiconductor integrated circuit comprising:

at least four separate power supply lines; and

at least two transistors for switching between said at least four power supply lines,

wherein first, second and third power supply lines of said at least four power supply lines are arranged side-by-side in that order,

wherein said at least two transistors include first and second transistors respectively placed in a gap between said first and second power supply lines and a gap between said second and third power supply lines, said first and second transistors being formed on opposite sides of said second power supply line,

wherein said first and second transistors are thin-film transistors on an insulation substrate other than a glass substrate or a semi-conductor substrate, and

wherein said first transistor switches between said first and second powers supply lines and said second transistor switches between said second and third powers supply lines.

32. (currently amended) A layout of a semiconductor integrated circuit, comprising:

at least four separate power supply lines; and

at least two transistors for switching between said at least four power supply lines,

wherein first, second and third power supply lines of said at least four power supply lines are arranged side-by-side in that order,

wherein said at least two transistors include first and second transistors respectively placed in a gap between said

first and second power supply lines and a gap between said second and third power supply lines, said first and second transistors being formed on opposite sides of said second power supply line,

wherein at least one of said at least four power supply lines extends straight to an external connection terminal and is connected to said external connection terminal.